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TRB3 - FPGA BASED, UNIVERSAL READOUT BOARD FOR PHYSICS EXPERIMENTS

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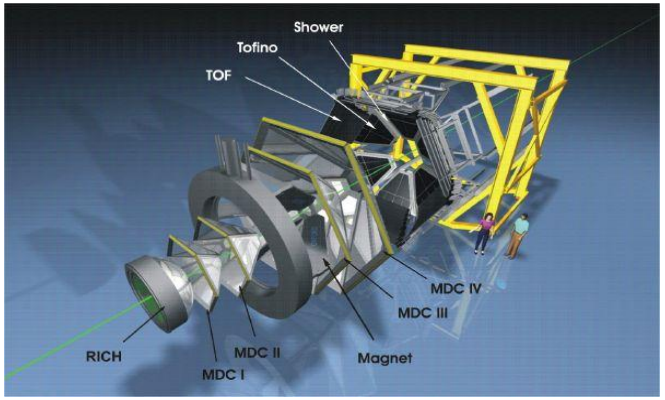
Plan

1. Predecessor: TRBv2
2. TRBv3 key features
3. TDC in FPGA implementation
4. GbE connectivity
5. Addon boards concept
6. Recent projects
7. Summary

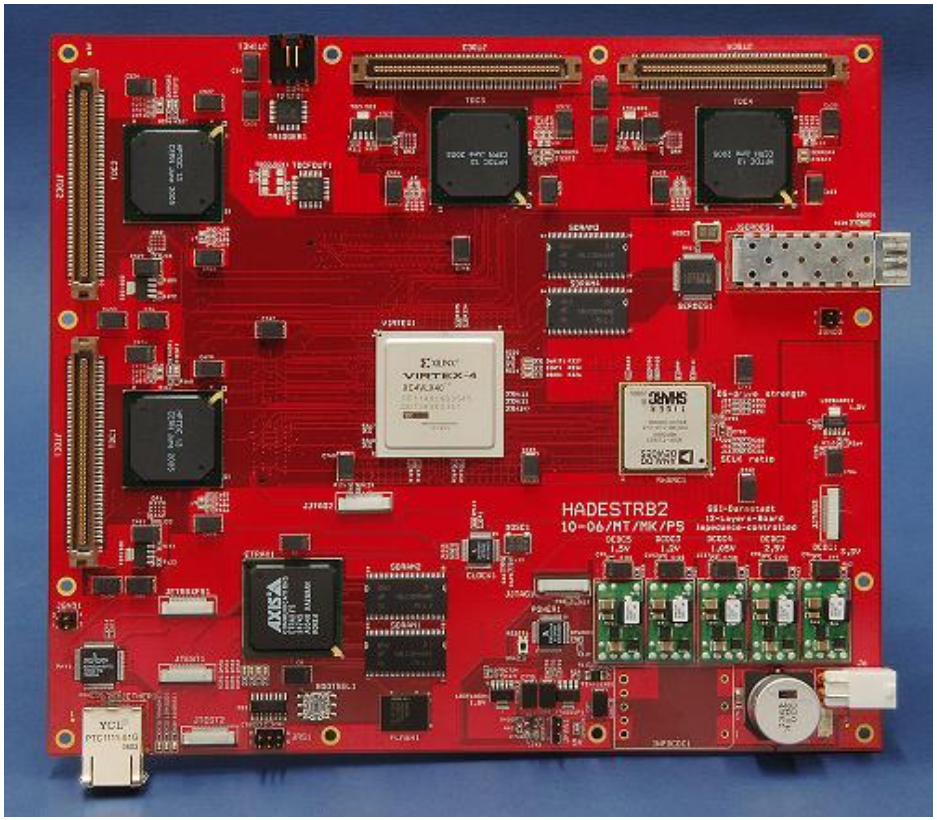
Predecessor: TRBv2

- Main user: HADES experiment at GSI, Darmstadt
  - Successfully used in many beatimes
  - Time measurement – HPTDC
    - 128 channels – 30 ps resolution
    - 32 channels – 13 ps resolution
  - Motherboard
    - Supports many Addon boards
  - Slow control
    - ETRAX processor
- Used in many different projects:
  - Detectors prototypes
  - PET projects



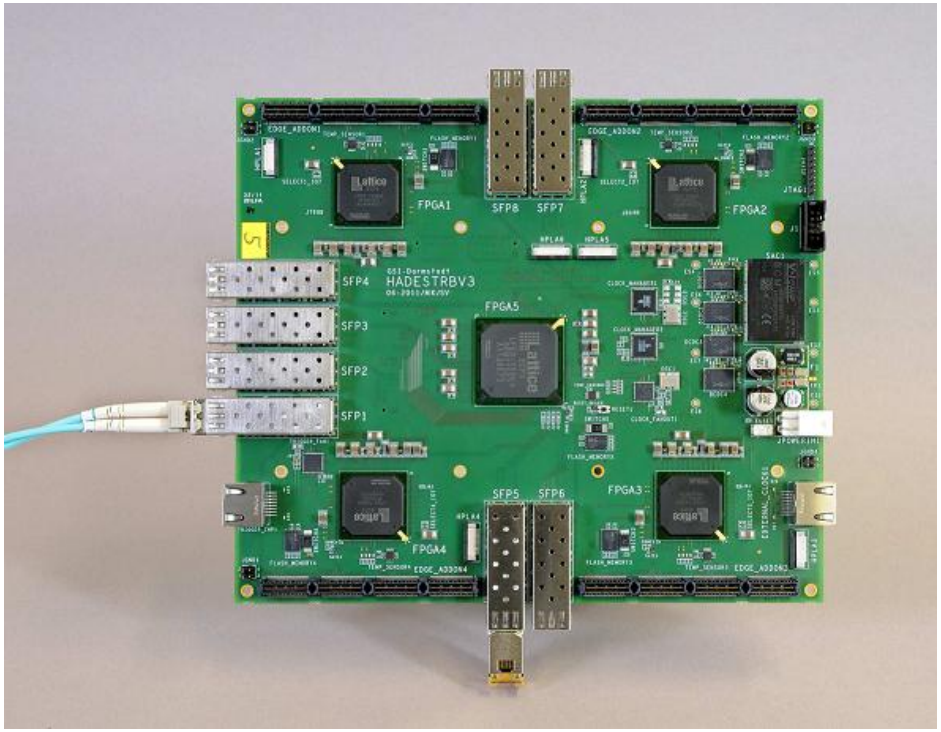
Predecessor: TRBv2

- 4x HPTDC
  - 32 channels each
  - Up to 13ps resolution
- 1x Xilinx Virtex4 FPGA
  - TDC readout
- 1x ETRAX
  - Interface for slow control
- 1x 2,5Gbps Optical link
  - Data output
  - Connection to the larger system
- 1x Sharc DSP
- 1x RJ45
  - Interface to network
- 1x Addon connector
  - Extension board slot
- 1x Reference time input



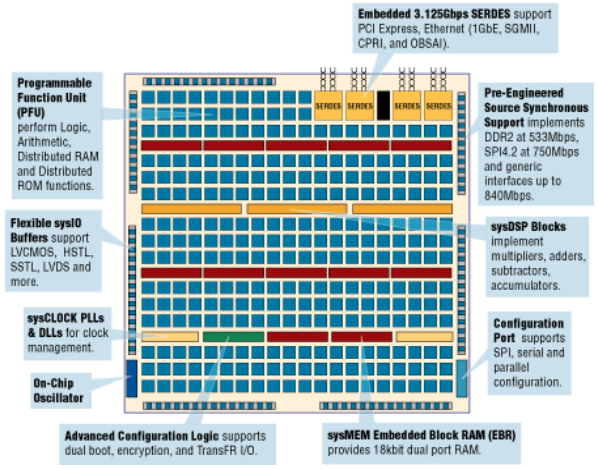
TRBv3 – Key features

- 5x Lattice ECP3 150 FPGAs
  - 4 edge devices
  - 1 central
  - Flash ROMs for each
- 8x 3.2GBps optical links
- 4x 208pin QMS connectors
  - Small Addons
- 1x 106pin connector
  - Large Addon
- Hardware trigger input



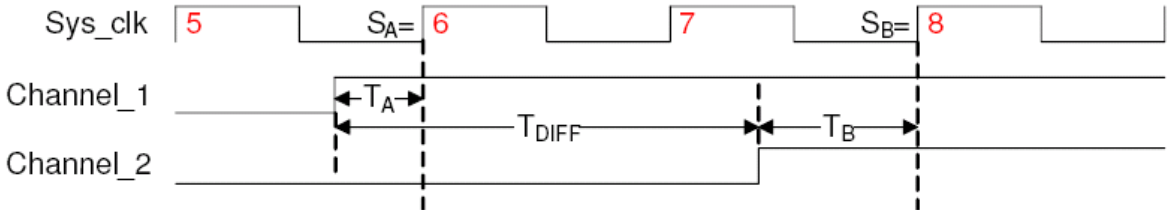
TDC in FPGA implementation

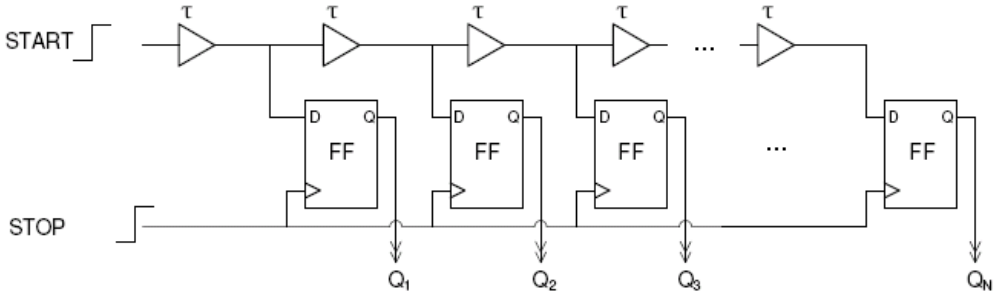
- Field Programmable Gate Arrays
  - Reconfigurable programmable logic devices
  - Parallel processing
  - High clock frequency
  - Memory blocks
  - DSP blocks
  - SERDES units
  - Hard/soft core CPU

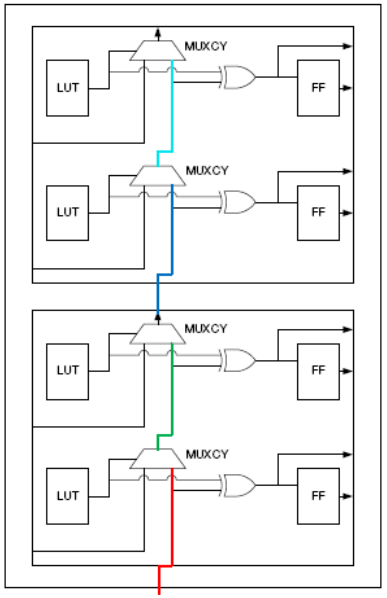


TDC in FPGA implementation

- No additional devices
- Precise time measurement (< 14ps resolution)
- High channel density (up to 64 channels per FPGA)
- 40MHz hit rate per channel
- Configurable by the end user (resolution in trade of channel number)

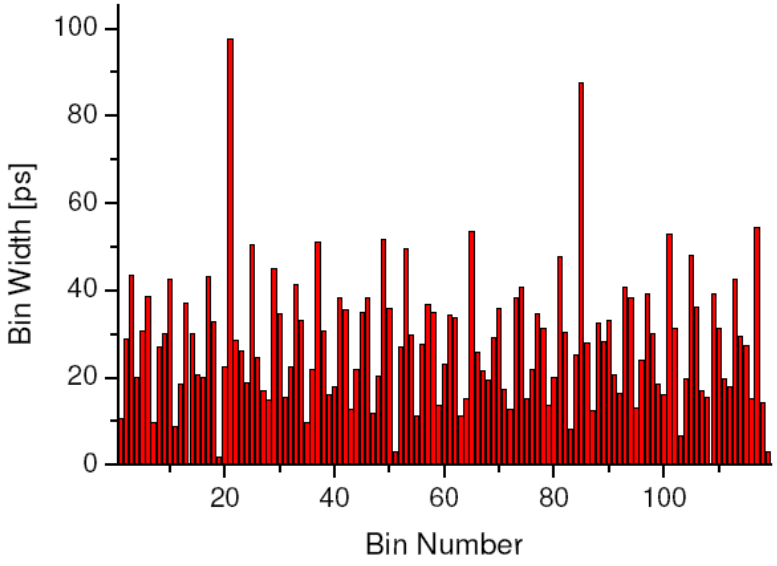


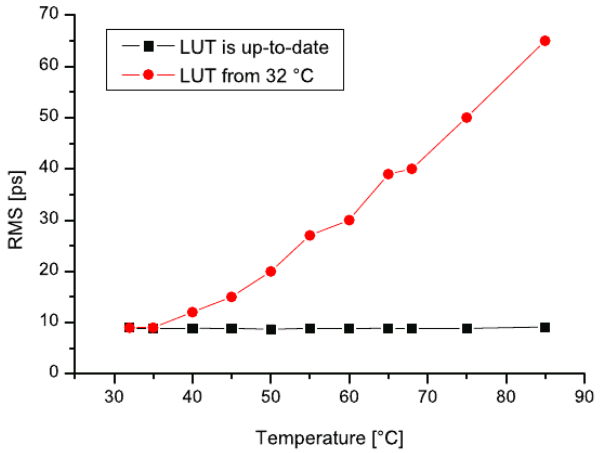


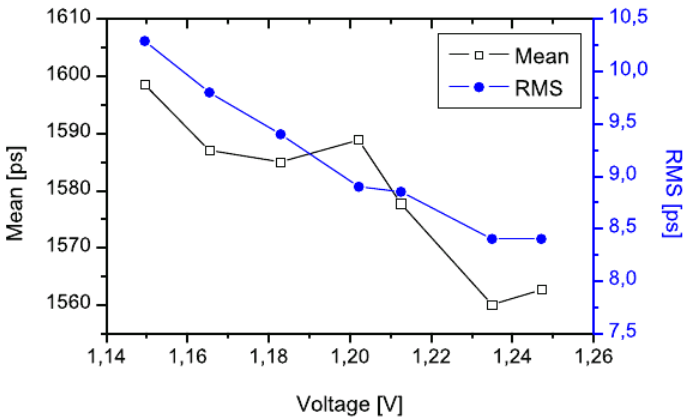


TDC in FPGA implementation

- Arrays/block boundaries – „Ultra Wide Bins”
- Sensitive to temperature and voltage variations
- Values vary between 3 ps – 100 ps
- PAR constraints very important
- Calibration needed

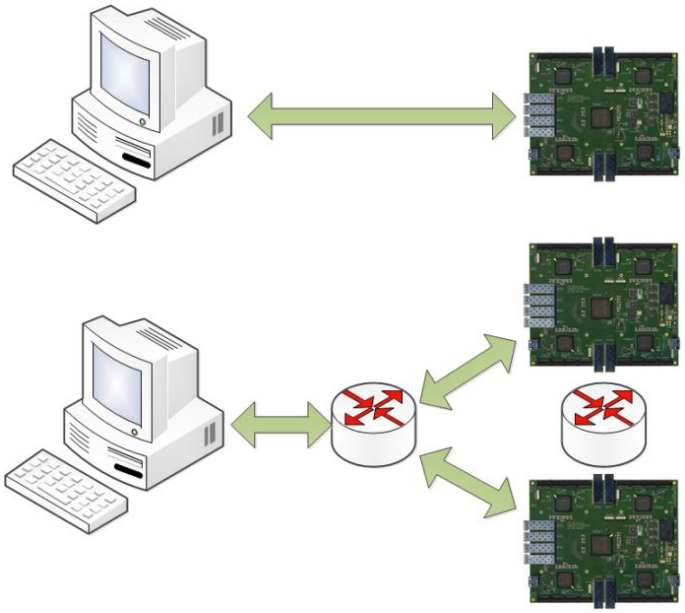






GbE connectivity

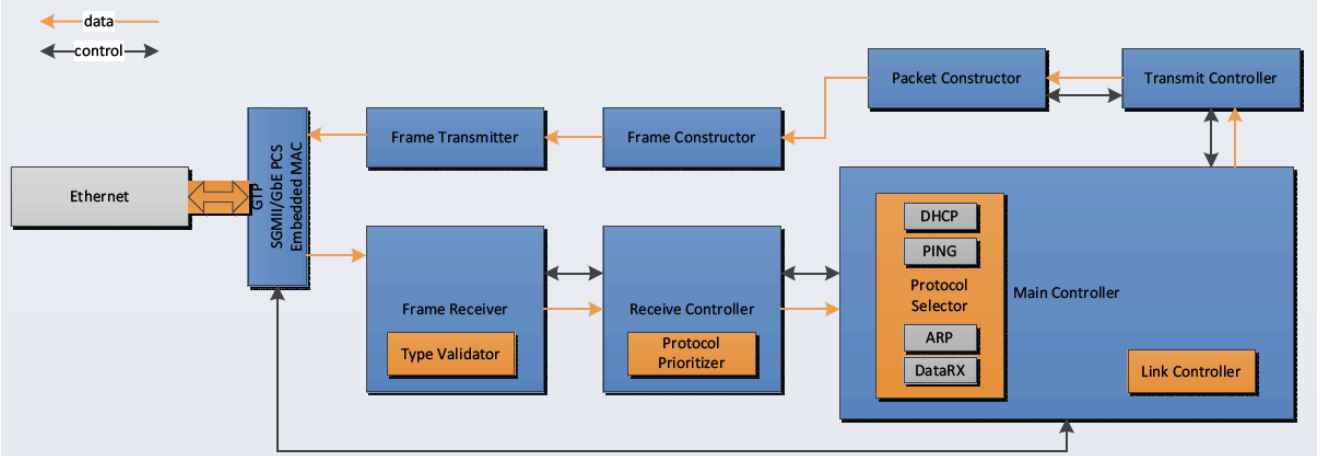
- TRBv3 designed to be used as:
  - Stand-alone measurement device
  - Part of a complex system



- Different communication solutions:
  - Based on 3.2GBps optical links
  - Links configured by groups of 4
  - Managed by central FPGA
  - Transmission of collected data
  - Control of the board or of the whole system

GbE connectivity

- Board management and data transmission
  - Gigabit Ethernet link
  - Full Duplex
  - Up to 118 MBps
  - Basic protocols (IP, UDP, ARP, DHCP, ICMP, Custom protocols)
  - Autonegotiation + network address acquisition
  - VLAN
  - Jumbo frames
  - Address filtering



Giagbit Ethernet with higher level protocols FPGA implementation

GbE connectivity

- Replacement for ETRAX
  - Slow control
- Network hub
  - Gathering of data from endpoints using custom protocols
  - Transmission to event builders via GbE
- Network traffic generator
  - Generation of personalized traffic in variety of protocols

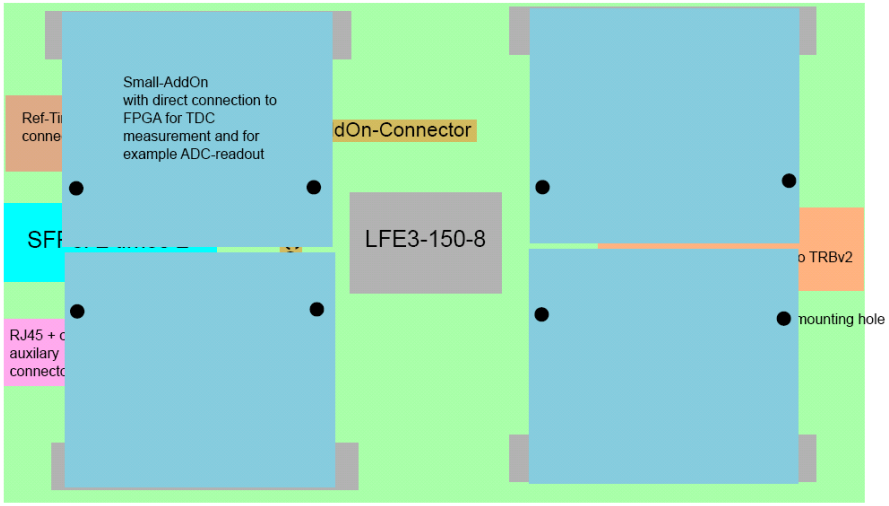
Addon boards concept

- 4x 208 pin connectors
- 1x 106 pin connector

- Features:
  - Data transfer
  - 3,3V and 6V power supply

- Addon boards:
  - Input signal converters
  - Front-end modules
  - Additional measurement devices
  - Input / output extensions

TRBv3 with small AddOns to cope with many applications.



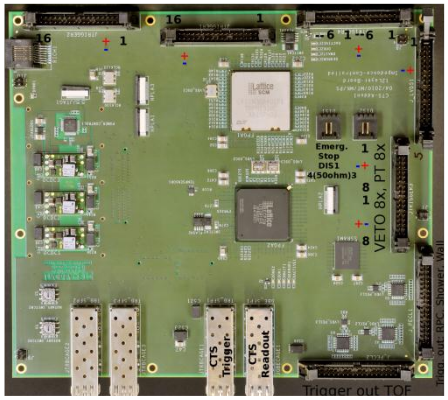
- Applications:
  - Measurement
  - Trigger module
  - Network hub

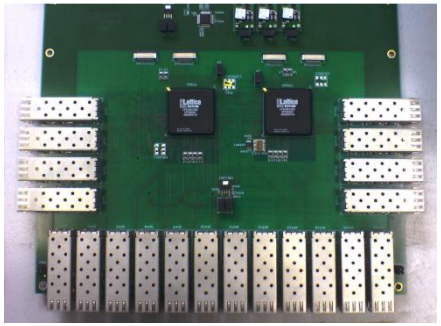
Addon boards concept

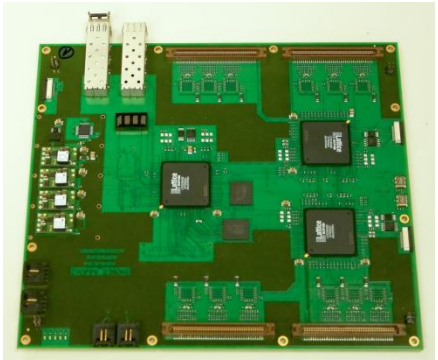
- Small addons:
  - HUB module
    - Additional 6x 3.2GBps optical links
  - Central Trigger System module
    - Many input and output LVDS ports
  - ADC module
    - Board prototype, basic values: 2 channels, 10MSps, 6bit
    - Uses TDC on FPGA

Addon boards concept

- Large addons (used already with TRB2):
  - Central Trigger System module
  - HUB module
    - 20x 3.2GBps optical links
  - ADC module
    - 12x 8 channel, 40MSps, 10b ADC
  - NINO module
    - 128 channels TOT

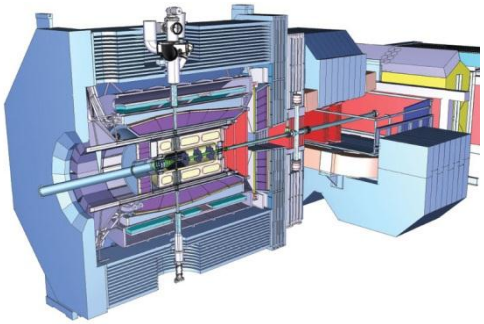


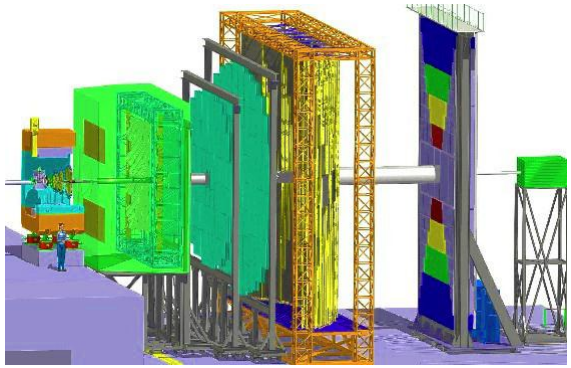




Recent projects

- Replacement of TRB2 in HADES (GSI)
- PANDA (GSI) detectors prototypes:
  - Disc and Barell DIRC
  - Straw Tube Tracker
- CBM (GSI) detector prototypes:
  - MVD
  - Calorimeter
- Positron Emission Tomography
  - TOF project in Cracow
  - RPC project in Coimbra
- Many other





Summary

- Versatile solution for different kind of measurements
- Flexible integration with existing DAQ systems thanks to communication features
- Board produced and under intensive testing
- Already planned to be used in many upcoming experiments